REMARKS

This application has been reviewed in light of the Office Action dated July 1, 2004.

Claims 1, 3-6, 8-12, 14-16 and 18-26 are in the application. Claims 2, 7, 13 and 17 have been cancelled without prejudice. Claims 21-26 have been withdrawn from consideration by the Examiner as being directed to a non-elected invention. Claims 1, 4-6, 8, 12, 15, 16 and 18 have been amended to more particularly point out and distinctly claim the subject matter regarded as the invention. Claims 1, 12 and 21 are independent. Favorable review is respectfully requested.

The Examiner stated that the title of the invention was not descriptive. The title has been changed as suggested by the Examiner.

Claim 1 was objected to because of informalities; the Examiner stated that, in the recitation of "forming studs on one of the first layer and the second layer and a third layer on the other of the first layer and the second layer," the phrase "the other" should be changed to --one--. A step of forming a third layer is now explicitly recited, to further clarify that (a) studs are formed on one of the first layer and second layer, and (b) the third layer is formed on the other of those two layers; that is, the one of the first and second layer on which the studs were not formed. It is believed that the objection has been thereby overcome.

Independent claim 1 has been amended to incorporate the subject matter of claims 2 and 7. Claim 12 has been amended to incorporate the subject matter of claims 13 and 17. Claims 2, 7, 13 and 17 have accordingly been cancelled. Claims 4-6, 8, 15, 16 and 18 have been amended to avoid their depending from a cancelled claim.

Claims 1-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Pogge et al., IBM Microelectronics, "Bridging the Chip/Package Process Divide" (hereinafter Pogge et al.). The applicants respectfully submit that amended independent claims 1 and 12 are patentably distinct from the cited art, for the following reasons.

The present invention, as defined in claim 1, is directed to a method for fabricating an integrated structure. This structure includes a semiconductor device and connector structures for connecting the semiconductor device to a motherboard. A first layer is formed which has

conductors therein; the conductors connect to bonding pads. The bonding pads are spaced according to a required spacing of connectors to the motherboard. As taught in the specification (page 8, lines 17-21, and Figure 4A), the area occupied by the bonding pads is typically larger than the area occupied by the device. A support structure is attached to the first layer; the support structure surrounds the semiconductor device, and has an area corresponding to an area occupied by the bonding pads. In the first embodiment described in the specification, the support structure comprises stiffener 41 which surrounds chip 31 and occupies area 40 (the additional area required for the bonding pads, as shown in Figures 4A and 4B).

Claim 12 is similarly directed to a method for fabricating an integrated structure, in which a first layer has conductors connected to bonding pads spaced according to a required spacing of connections to a motherboard. A plurality of C4 connectors (formed on a second layer on a semiconductor device) are attached to the first layer. A support structure is formed on the first layer; the support structure surrounds the semiconductor device, and has an area corresponding to an area occupied by the bonding pads. In the second embodiment described in the specification, the support structure comprises stiffener 41 which surrounds chip 61 and occupies the additional area required for the bonding pads, as shown in Figures 6A, 6B and 6D.

It is thus a feature of the present invention that a support structure is formed which surrounds the semiconductor device, and which has an area occupied by the bonding pads (whose spacing is in accordance with the required spacing of connections to the motherboard). This feature is neither disclosed nor suggested by Pogge et al. Pogge et al. describes a transfer-and-join (T&J) process for interconnecting chips, by attaching those chips to an interconnect wiring layer using stud-via connections. This process is described in the "Discussion" section and illustrated in Figure 5. The applicants wish to point out that there is no discussion or illustration of bonding pads which occupy a larger area than that of the chips. Indeed, the nine illustrations in Figure 5 show only an area occupied by two chips connected by the T&J process, and offer no information regarding anything surrounding the chips. The bonding pads shown in these illustrations are confined to an area corresponding to the

connected chips, as opposed to a larger area. There is thus no suggestion that the area occupied by the bonding pads would correspond to any area surrounding the chips. Furthermore, there is no discussion or suggestion of bonding pads whose spacing is in accordance with a required spacing of connections to a motherboard. The only suggestion of connections to another level of packaging is in Figure 5.9, which shows two C4 interconnects attached to bonding pads. (*See* "Discussion" section, second paragraph.) It is noteworthy that in Figure 5.9, the C4 interconnects are located within the area occupied by the chips. There is thus no disclosure or suggestion of a support structure which surrounds a chip, as in the present invention. There is furthermore no disclosure or suggestion that the support structure have an area corresponding to an area occupied by the bonding pads.

Since the above-described feature of the invention (defined in claims 1 and 12) is not disclosed by Pogge et al., the present invention is not anticipated by that reference.

The other claims now under consideration in this application are each dependent from one or the other of the independent claims discussed above and are therefore believed patentable over Pogge et al. for the same reasons. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

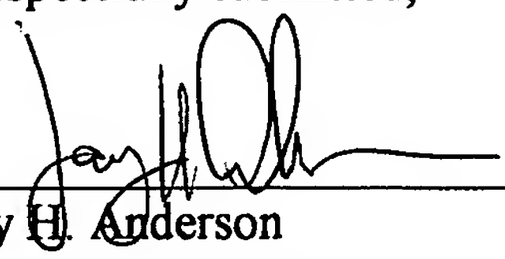
Claims 1-20 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 of U.S. Pat. No. 6,444,560.

A Terminal Disclaimer with respect to U.S. Pat. No. 6,444,560, in compliance with 37 C.F.R. § 1.321(c), is submitted herewith. The double patenting objection is believed to be thereby overcome. The Commissioner is authorized to charge the sum of $ 110.00, to cover the terminal disclaimer fee under 37 C.F.R. § 1.20(d), to Deposit Account 09-0458. Any deficiency or overpayment of this or any other required fees should likewise be charged or credited to Deposit Account 09-0458.

In view of the foregoing amendments and remarks, the applicants respectfully request favorable reconsideration and early passage to issue of the present application.

The applicants' undersigned attorney may be reached by telephone at (845) 894-3667. All correspondence should continue to be directed to the below listed address.

Respectfully submitted,



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